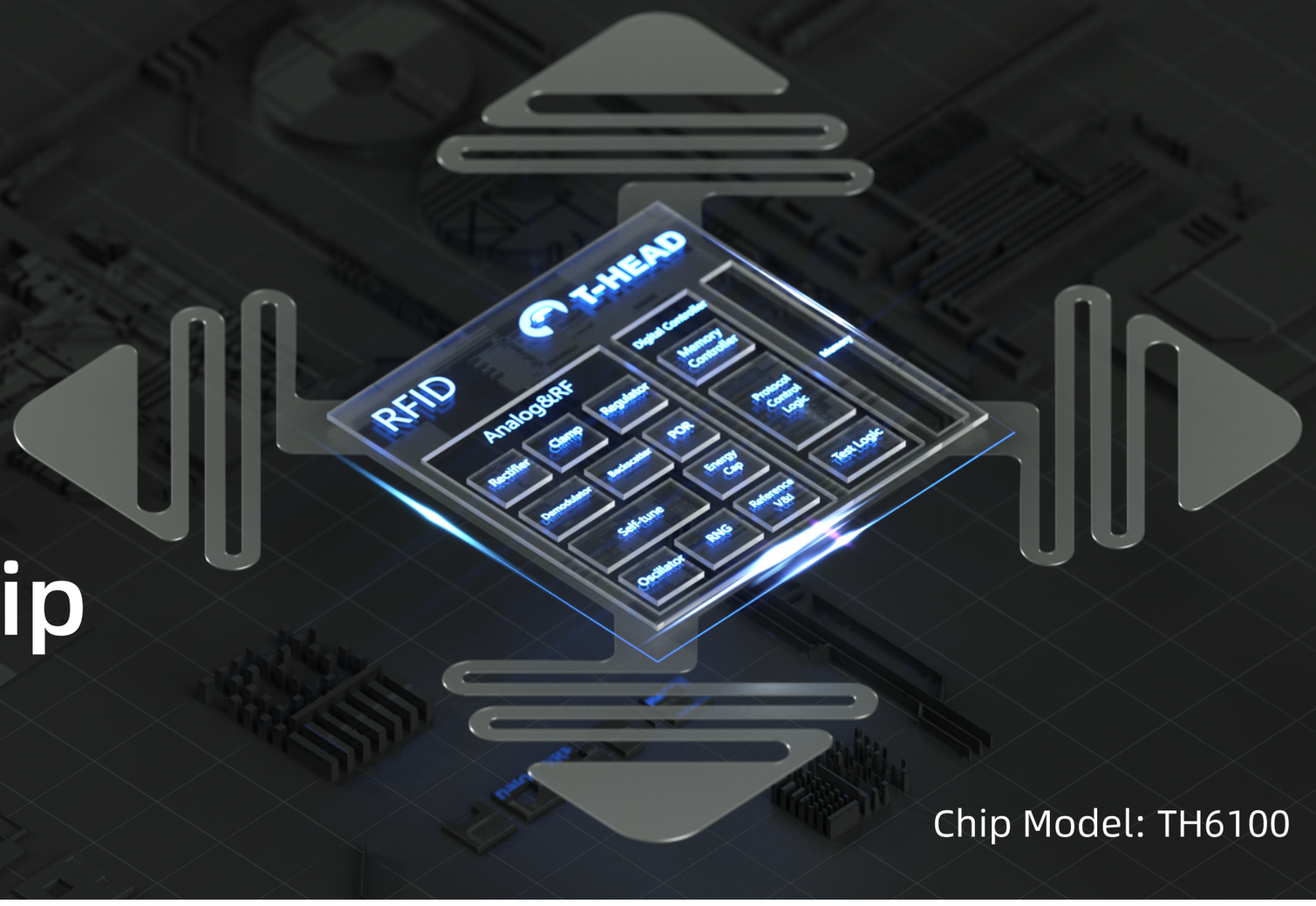
T-HEAD

Yuzhen600
UHF RFID Tag Chip



Chip Model: TH6100

【Revision】

Document ID	Release Date	Document Status
1.0	2021/9/26	The architecture diagram is updated.
1.1	2022/5/11	The name is updated.
1.2	2022/5/20	The read sensitivity is updated.

【List of Abbreviations】

Abbreviations	Description
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DSB-ASK	Double Side Band-Amplitude Shift Keying
DC	Direct Current
EAS	Electronic Article Surveillance
NVM	None Volatile Memory
EPC	Electronic Product Code (containing Header, Domain Manager, Object Class and Serial Number)
FM0	Bi phase space modulation
IC	Integrated Circuit
PIE	Pulse Interval Encoding
RF	Radio Frequency
UHF	Ultra High Frequency
TID	Tag Identifier

【Contents】

Revision ---- 01

List of Abbreviations ---- 01

1 Chip Overview ---- 04

2 Characteristic Parameters ---- 04

2.1 Characteristic Parameters ---- 04

3 Application Scenarios ---- 04

3.1 Target Markets ---- 04

4 System Block Diagram ---- 04

5 Pin Information ---- 05

5.1 Pin Information Description ---- 05

6 Wafer and Chip Parameters ---- 06

6.1 Wafer and Die Specifications ---- 06

7 Function Description ---- 07

7.1 Air Interface Standard ---- 07

7.2 Energy Transfer ---- 07

7.3 Data Transmission ---- 07

7.3.1 Reader-to-Tag Link ---- 07

7.3.2 Tag-to-Reader Link ---- 07

7.4 Memory ---- 07

7.4.1 EPC Area ---- 08

7.5 Special Description ---- 08

7.5.1 Session ---- 08

7.5.2 Memory bank ---- 09

【Contents】

7.5.3 EBV ---- 09

7.6 Self-Tune ---- 09

7.7 Wide-Pad Connection Scheme ---- 09

7.7.1 Single-Port Connection ---- 09

7.7.2 Dual-Port Connection ---- 10

8 Limit Parameters ---- 10

9 Performance Parameters ---- 11

【1 Chip Overview】

T-Head TH6100 is a low-power, high-performance UHF RFID tag chip that complies with the EPC Global Class-1 Generation-2 UHF RFID protocol. With the ultra-low power circuit design, dual-port antenna and fully automatic impedance tuning, it is particularly suitable for a variety of application scenarios such as smart retail, smart logistics, air parcel tracking, and inventory management.

【2 Characteristic Parameters】

【2.1 Characteristic Parameters】

- Compliant with the EPC Global Class-1 Generation-2 UHF RFID protocol specifications
- Read sensitivity up to -21dBm
- Key features
  - ➢ Self-tune support for complex applications
  - ➢ Dual-port omnidirectional antenna and the tag read directionality is not sensitive
  - ➢ Wide-PAD package, providing reliability of antenna and chip Bonding connection
- ESD: HBM ±2kV, CDM ±500V
- Operating Temperature: -40°C to +85°C
- Memory:
  - ➢ 96-bit factory pre-programmed EPC area (read-only)

【3 Application Scenarios】

【3.1 Target Markets】

- Smart logistics
- Retail
- E-commerce
- Supply chain
- management
- Air parcel tracking

【4 System Block Diagram】

The TH6100 chip consists of three main modules, as shown in Figure 1.

- Analog & RF module
- Digital controller
- Memory

The analog & RF module provides a stable power supply and demodulates the data received from the reader, which is then processed by the digital controller. In addition, the backscatter in the analog & RF module sends the modulated data back to the reader. The digital controller includes protocol control logic, memory controller and test logic and is responsible for processing the EPC protocol and completing the communication with the reader.

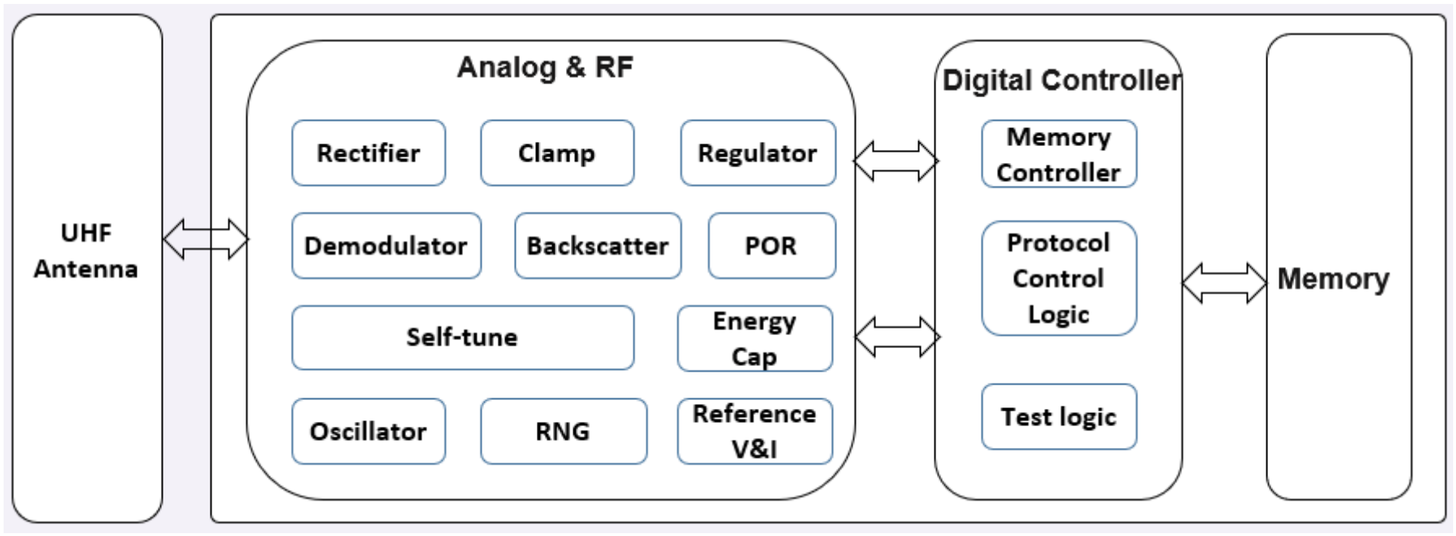


Figure 1 TH6100 functional block diagram

【5 Pin Information】

TH6100 uses Wide-Pad package technology, and the overview is shown in Figure 2.

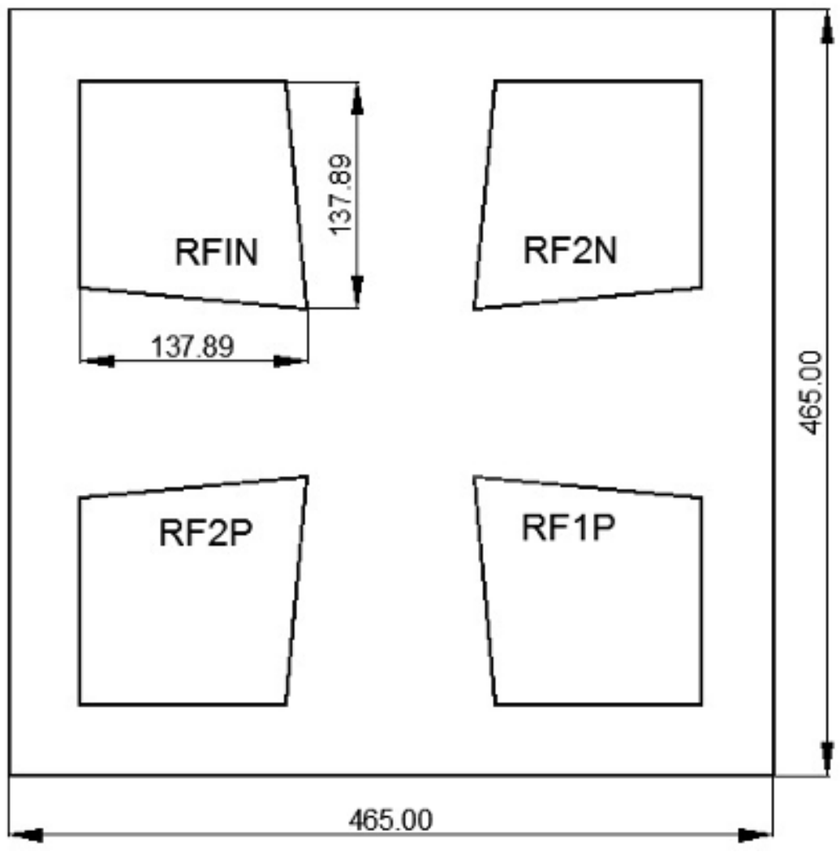


Figure 2 TH6100 package overview

【5.1 Pin Information Description】

Table 1: TH6100 pin information

Symbol	Description
RF1N	Port1 RF negative input
RF1P	Port1 RF positive input
RF2N	Port2 RF negative input
RF2P	Port2 RF positive input

【6 Wafer and Chip Parameters】

The TH6100 chip has a typical thickness of 125 μm, including a 10 μm Polyimide layer. The introduction of the Polyimide layer significantly reduces the coupling between the antenna and the chip, which improves the chip performance to a certain extent.

【6.1 Wafer and Die Specifications】

Table 2: TH6100 wafer and chip main specifictions

Wafer	Specification
Diameter	200 mm (8")
Thickness	125 μm ± 15 μm
Number of pads	4
Pad location	placed in chip corners
Wafer backside	
Material	Si
Chip dimensions	
Die size excluding scribe	0.465mm*0.465mm = 0.216 mm^2
Scribe line width	x-dimension = 25 μm
	y-dimension = 25 μm
Passivation on front	
Type	Sandwich structure
Material	PE-Nitride (on top)
Thickness	1.75 μm total thickness of passivation
Polyimide spacer	10 μm ± 2 μm
Au pads	
Pad material	> 99.9 % pure Au
Pad height	3 μm ± 1 μm
Bump size	138um X 138um

【7 Function Description】

【7.1 Air Interface Standard】

TH6100 complies with the specification "EPCTM Radio-Frequency Identity Protocols Generation-2 UHF RFID, RFID Air Interface Specification, 860 MHz to 960 MHz Communication Protocol, Version 2.1".

TH6100 supports all necessary commands contained in the Select and Inventory command groups, including Select, Query, Query_Adj, Query_Rep, ACK, and NAK.

【7.2 Energy Transfer】

The reader provides the tag with the UHF RF field and the tag antenna receives energy from the RF field and transmits the energy to the chip. In order for the chip to get the maximum power transfer, the impedance of the antenna and the chip need to be matched.

【7.3 Data Transmission】

【7.3.1 Reader-to-Tag Link】

The reader transmits information to the TH6100 tag by modulating the UHF RF signal. The TH6100 tag is passive and receives information and energy from this RF signal. The TH6100 tag chip supports demodulation of 3 modulation formats, DSB-ASK, SSB-ASK and PR-ASK, using PIE encoding.

【7.3.2 Tag-to-Reader Link】

After sending a valid command, the reader receives the information from the TH6100 tag by sending an unmodulated RF carrier and listening for a backscatter response. TH6100 backscatters by switching the reflection coefficient of its antenna between two states based on the data sent. The encoding format for responding to reader commands is baseband FM0 or Miller Subcarrier.

【7.4 Memory】

The TH6100 tag chip uses non-volatile memory technology and is specifically optimized for RFID applications. The overall memory size is 192 bits and the memory content will be programmed before delivery. The mapping is shown in Table 3.

Table 3: TH6100 memory map

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR0	System configuration															
ADDR1	System configuration															
ADDR2	System configuration															
ADDR3	System configuration															
ADDR4	EPC[95:80]															
ADDR5	EPC[79:64]															
ADDR6	EPC[63:48]															
ADDR7	EPC[47:32]															
ADDR8	EPC[31:16]															
ADDR9	EPC[15:8]								EPC[7:0]							
ADDR10	Stored CRC[15:0]															
ADDR11	System configuration															

【7.4.1 EPC Area】

According to the EPC Global C1 Gen2 specification, the EPC contains a 16-bit cyclic redundancy check word (CRC16) at memory addresses 0x00 to 0x0F and 16 protocol control words (PC) at memory addresses 0x10 to 0x1F. The protocol control field contains 5-bit EPC length, 1-bit user memory indicator (UMI = 0), 1-bit extended protocol control indicator, and 9-bit numbering system identifier (NSI). The TH6100 chip supports an EPC length of 6 words, i.e. the PC value is fixed at 0x3000.

【7.5 Special Description】

【7.5.1 Session】

TH6100 supports SL, S0, S1, S2, but not S3. Any command that uses S3 as a parameter will considered invalid. Invalid commands do not change any state.

【7.5.2 Memory bank】

TH6100 only supports the EPC area. Any command that uses the TID area, user area, or reserved area as a parameter will be considered invalid. Invalid commands do not change any state.

【7.5.3 EBV】

As TH6100 has 96 bits of EPC data, it does not support the Extensible Bit Vector (EBV) in the pointer parameter of the SELECT command. The pointer parameter of the SELECT command is a fixed length of 8 bits. The value of the pointer should be between 0x00 and 0x7F. When the MSB of the pointer is 1 (in binary format), the command will be considered invalid. Invalid commands do not change any state.

【7.6 Self-Tune】

TH6100 has an self-tune mechanism that adapts the chip sensitivity to its maximum in a variety of complex scenarios. This adjustment will be performed at startup and will be selected between eight different input capacitance values (capacitance step ~35fF). This function is enabled by default.

【7.7 Wide-Pad Connection Scheme】

The Wide-Pad design of TH6100 allows for a more reliable connection to the antenna. This Wide-pad design allows greater freedom in terms of processing accuracy. The recommended RF port configuration is shown in Figure 3, with 2 configurations for the port connection to the antenna.

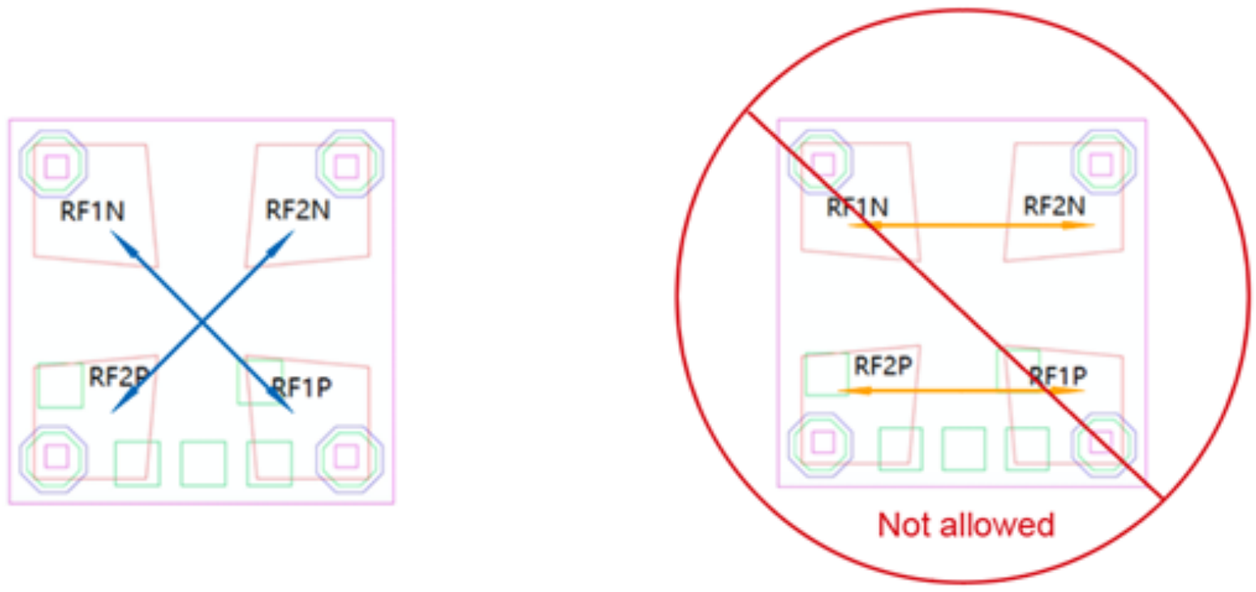


Figure 3 Connection method between chip and antenna

【7.7.1 Single-Port Connection】

In the single-port configuration, the signal acts on one of the TH6100 antenna ports. The antenna ports are defined as: RF1P and RF1N are PORT1, and RF2P and RF2N are PORT2. The antenna needs to be connected to a pair of diagonal PADs, as shown in Figure 4. Since the two ports are identical in electrical performance, either pair can be used.

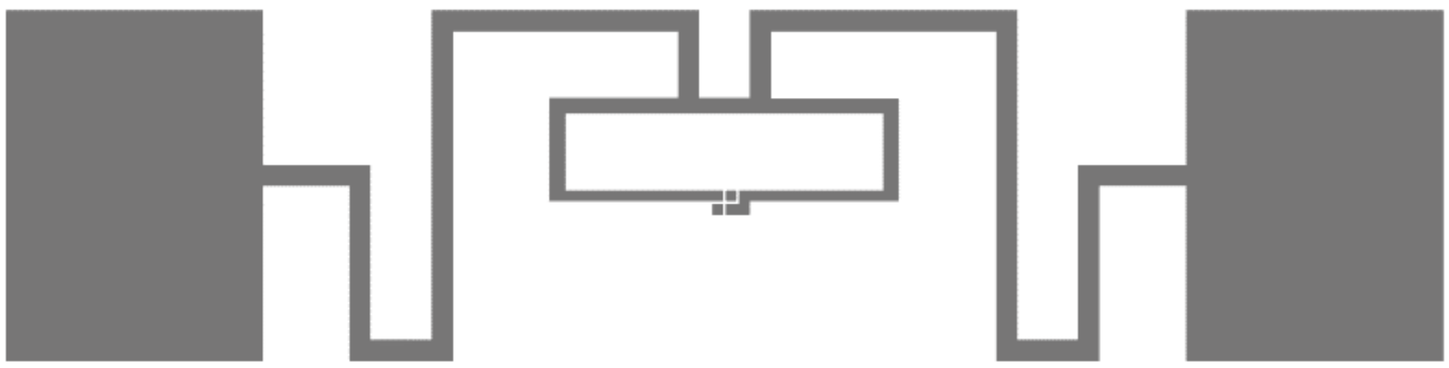


Figure 4 Single-port antenna design

【7.7.2 Dual-Port Connection】

The TH6100 chip supports dual-port connection. This configuration is the focus of omnidirectional antenna technology and increases read rates by improving tag directionality. Figure 5 shows the reference design for a dual-port tag antenna.

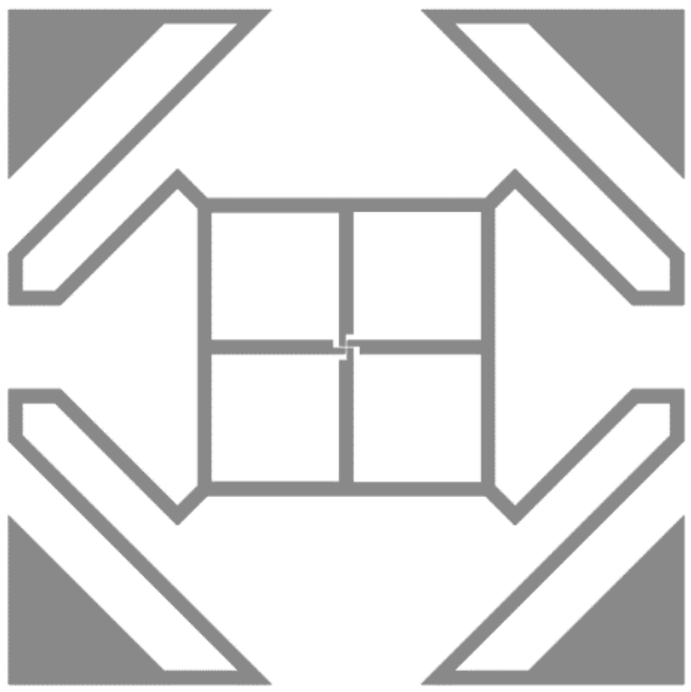


Figure 5 Dual-port antenna design

【8 Limit Parameters】

Table 4: TH6100 chip limit parameters

Symbol	Parameter	Conditions	Min	Max	Unit
Bare die limit value					
T_{stg}	Storage temperature	NA	-55	+125	°C
T_{amb}	Operating temperature	NA	-40	+85	°C
V_{ESD}	ESD	human body model (HBM)	±2	-	kV
Pad limit value					
P_i	Input power	Max input power consumption, PORT1/PORT2 pad	-	100	mW

【9 Performance Parameters】

Table 5: TH6100 RF port characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	Input frequency			840	-	960	MHz
$P_{i(min)}$	Min RF input power	Single-port dipole antenna	[1]	-	-21	-	dBm
$P_{i(max)}$	Max RF input power	Max input power		-	-	20	dBm
C_i	Chip input capacitance	Chip parallel equivalence	[3][5]	-	1.05	-	pF
R_P	Chip resistance	Chip parallel equivalence	[2][5]	-	2.4	-	KΩ
Z	Chip impedance	RF operating frequency 915MHz	[4][5]	-	11.4-j165	-	Ω

[1] Assume tag sensitivity on a 2.15dBi gain dipole antenna
[2] Min operating power
[3] Self-tune center capacitor
[4] The antenna should match this impedance
[5] Assume 50 fF additional package capacitance

Table 6: TH6100 memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Memory characteristics						
t_{ret}	Retention time	$T_{amb} \leq 55℃$	10	-	-	year