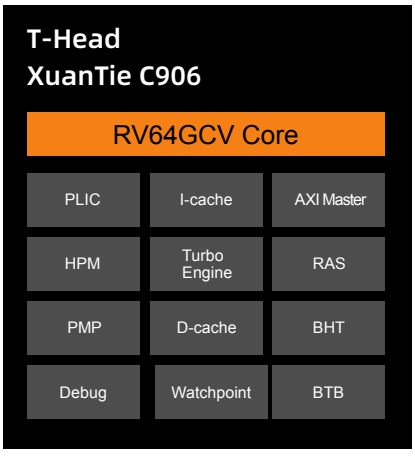
T-Head XuanTie C906

High energy-efficient, low cost RV64 compatible processor

Overview

The C906 procesor is based on the RV64GCV instruction set and includes customized arithmetic enhancement extension, bit manipulation extension, load store enhancement extension and TLB/Cache operations enhancement extension. The processor adopts a state of the 5-8 stages in-order pipeline. The C906 supports the Sv39 virtual address system with custom page attribute extensions. In addition, C906 includes standard CLINT and PLIC interrupt controllers, supports RV-compatible performance monitors.

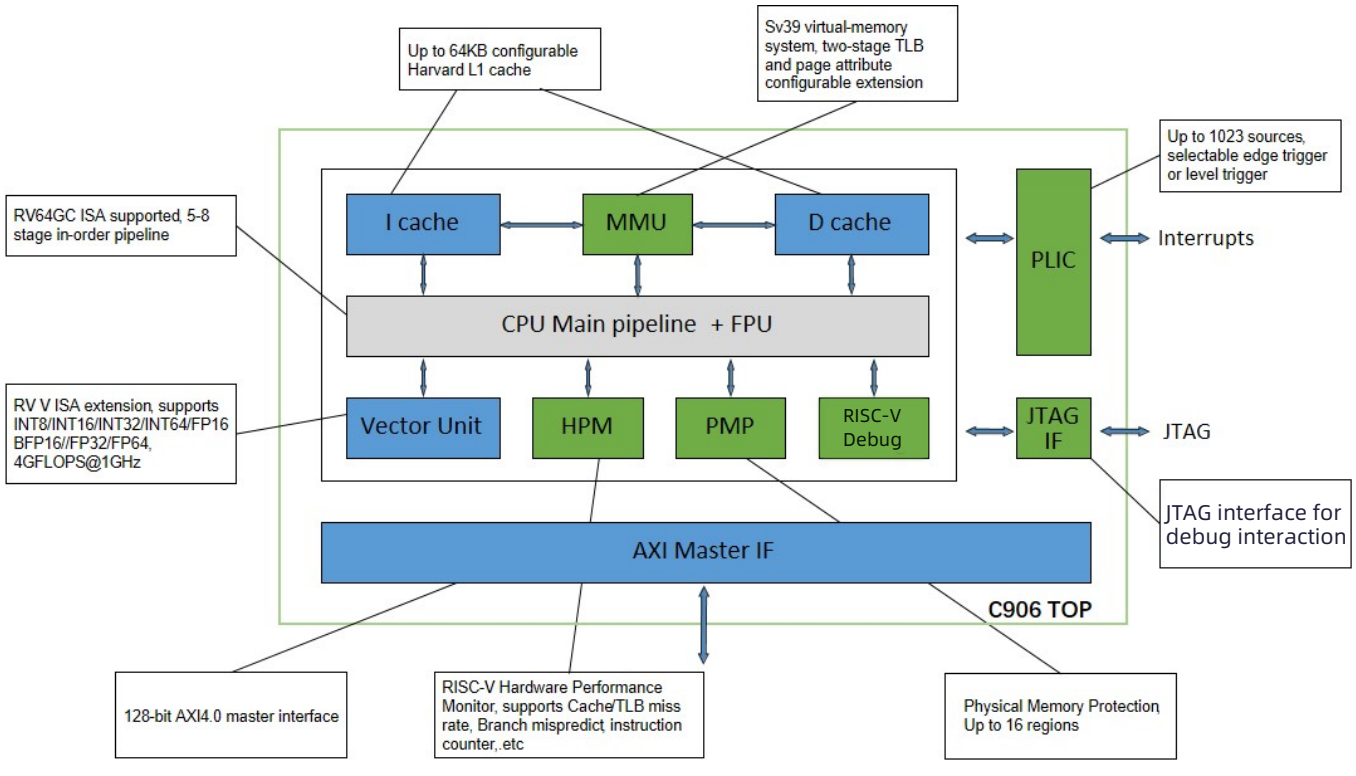


Features

Feature	Description
Architecture	RV64GCV
Floating-point Unit	Support RISC-V F, D instruction extension Support IEEE 754-2008 standard
Vector Unit	Support RISC-V V instruction extension（configurable），vector register width 128bit，element size support 8/16/32/64bit，support half precision.
Master Bus interface	AXI4.0 128-bit
Instruction Cache	Up to 64KB（configurable）
Data Cache	Up to 64KB（configurable）
Interrupt controller	Flexibly configurable Platform-Level Interrupt Controller (PLIC) for supporting wide range of system event scenarios
T-Head turbo instruction	Support
Physical Memory Protection (PMP)	Up to 16 regions

- **Applications**
  - Surveillance
  - Artificial intelligence

- **Interfaces**
  - Master AXI (M-AXI)
  - RISC-V Debug (JTAG)
  - Interrupt
  - Power control



Xuantie C906 Components

Memory sub-system

The C906 has up to 64KB instruction and data cache.

➢ The L1 instruction memory system has the following key features:

◇ VIPT, two-way set-associative instruction cache.
◇ Fixed cache line length of 64 bytes.
◇ FIFO cache replacement policy.

➢ The L1 data memory system has the following features:

◇ VIPT, four-way set associative L1 data cache.
◇ Fixed cache line length of 64 bytes.
◇ FIFO cache replacement policy.
◇ 128-bit read interface.

Memory Management Unit (MMU)

◇ Sv39 virtual memory systems support.
◇ 10-entry fully associative I-uTLB/D-uTLB.
◇ Up to 512-entry 4-way set-associative shared TLB.
◇ Hardware page table walker.
◇ Virtual memory support for full address space and easy code/data sharing.
◇ Support for full-featured OS such as Linux.
◇ Hardware for fast address translation.
◇ Page table entries are extended for additional attributes.

Physical Memory Protection (PMP)

- 16 regions basic read/write/execute memory protection with low cost.

Platform-Level Interrupt Controller (PLIC)

- Support multi target interrupt control
- Up to 1023 PLIC interrupt sources
- Up to 32 PLIC interrupt priority levels
- Up to 8 PLIC interrupt targets
- Selectable edge trigger or level trigger

Float Point Unit (FPU)

- RISC-V F and D extensions
- Support half/single/double precision
- Fully IEEE-754 compliant
- Does not generate floating-point exceptions
- User configurable rounding modes

Branch predictor

- Branch Target Buffer (BTB) and Branch History Table (BHT) to speed up control codes
- Return Address Stack (RAS) to speed up procedure returns

Hardware Performance Monitor (HPM)

- Program code performance tuning.

JTAG Debug

- Support RISC-V Debug Spec-0.14 version
- JTAG debug interface support several triggers
- Support software breakpoints
- Check and modify CPU register resource
- Single step or multi step flexibly supported
- High speed program downloading through JTAG

Vector Unit

- Support RISC-V Vector Extension 0.7.1-Workshop-Release
- Vector length is 128 bits
- Support 64 bits or 128 bits hardware data path width
- Support element INT8-INT64, FP16-FP64 and BFP16
- Up to 4GFLOPs (single core in 1GHz)

RV Compatibility with Custom Extensions

The C906 is fully compatible with the RV64GC instruction set and supports the standard M/S/U privilege program model. The C906 includes a standard 8-16 region PMP and Sv39 MMU, which is fully compatible with RISC-V Linux. The C906 includes standard CLINT and PLIC interrupt controllers, RV compatible HPM.

Configurations

Configuration	Options
FPU	No/SP+DP
Vector Unit	No/Yes(64/128 data path width)
L1 Data Cache	8KB/16KB/32KB/64KB
L1 Instruction Cache	8KB/16KB/32KB/64KB
Branch History Table	8Kb/16Kb
PMP	8/16 regions
PLIC	Up to 1023 interrupts
jTLB entry	128/256/512

Software Ecosystems

- ◇ Compiler, assembler, linker, debugger and binary tools are contributed to GNU and supported officially
- ◇ Linux kernel is contributed to Linux foundation and supported officially
- ◇ QEMU is contributed and supported officially
- ◇ Integrated Development Environment (CDS), compatible with Eclipse development
- ◇ Graphical profiling and statistical analysis tools base trace data（simulator）
- ◇ ICE, CK-Link Pro, high speed（1.1Mbytes/s）JTAG debug hardware

Linux System

C906 support official RISC-V Linux and its software applications ecosystem. eg: GNU toolchain, Fedora, Debian, buildroot and thousands of open source software based on Linux. T-Head will continue to make contributions on RISC-V architecture port in Linux ecosystem.

PPA

Performance	2.3 DMIPS/MHz (O2) 3.7 Coremark/MHz (O3)
Frequency	>1.0 GHz
Area	0.6 mm^2
Power	70 uW/MHz

UMC 22nm，RVT，9T library；
Dynamic power@tt 85c;
Frequency@ss,0.81v,m40c;
Area@typical configuration with 32KB I$, 32KB D$, 64bits Vector Unit