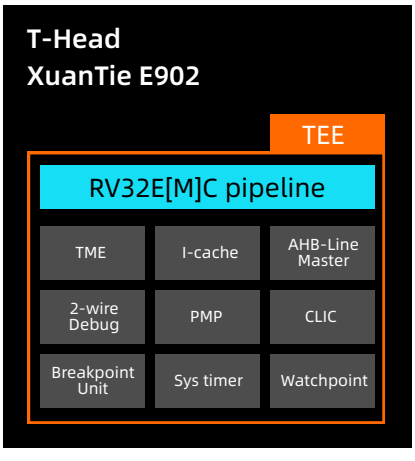
Overview

The T-Head XuanTie E902 is a fully synthesizable, microcontroller-class processor that compatible to the RISC-V RV32E[M]C ISA. It delivers ultra-low area and power aiming at the Low end MCUs and IoT applications.



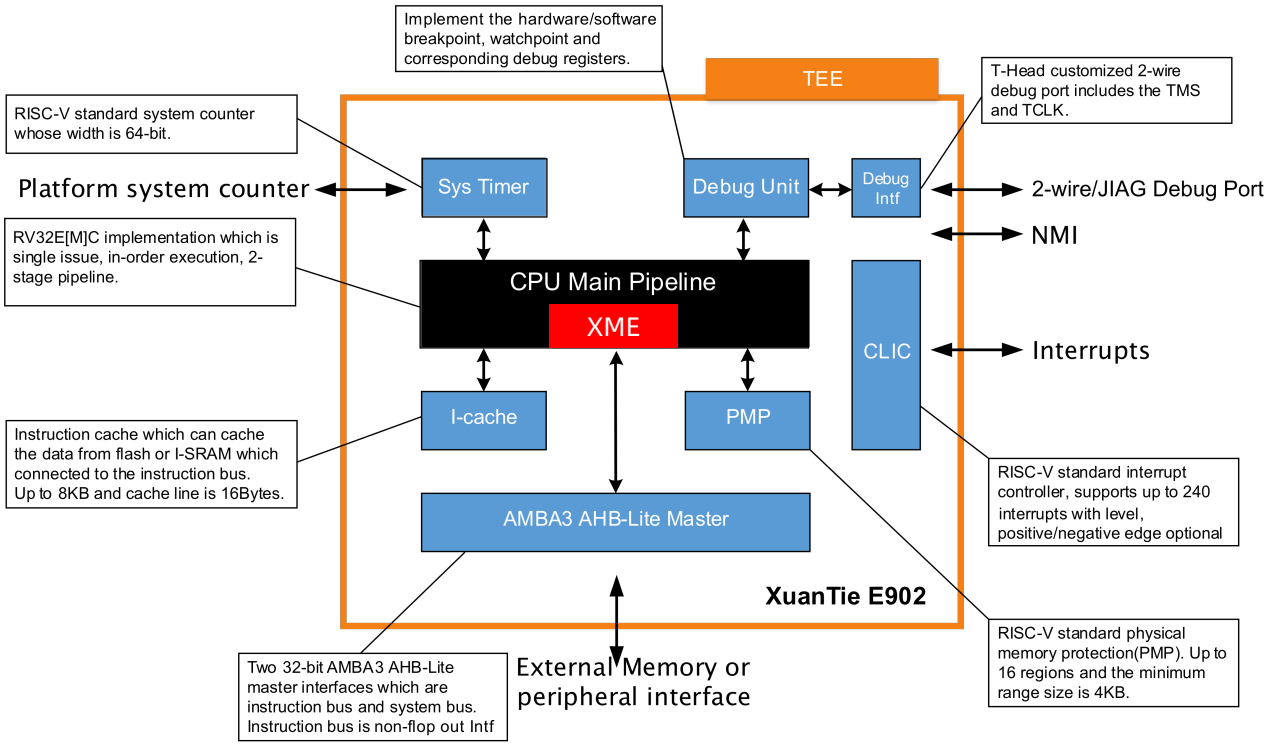
Features

Feature	Description
Architecture	RV32E[M]C
Bus interface	AMBA3 AHB-Lite 32-bit master
Pipeline	2-stages
Security	T-Head TEE technology (Optional)
Instruction cache	Up to 8KB (Optional)
Interrupts	Up to 240interrupts + Non-maskable interrupt (NMI)
Sleep modes	Sleep and deep sleep mode
Debug	2-wire/JTAG debug port, Hardware and software breakpoints

XuanTie E902 Components

- **Processor Overview**

The E902 processor adopts a 16/32 bits mixed instruction set and implements an energy-efficient 2-stage, single issue and in-order execution integer pipeline. Besides, E902 customizes four functional instructions and some extend CSRs to support the extensions.
The E902 processor supports the T-Head TEE technology which makes E902 suitable for the IoT application which needs to protect the sensitive information.



• Instruction Cache

E902 implements an optional instruction cache which can cache the data from the instruction bus such as Flash or I-SRAM. The instruction cache has following features:

◇ 2-way set-associative;
◇ FIFO cache replacement policy;
◇ Can be configured to 2KB/4KB/8KB.

• Physical Memory Protection (PMP)

The E902 processor has optional RISC-V PMP which allows machine and user privilege modes to access different address ranges. Only the machine mode has the authority to define the memory access permissions. If an authorized access is detected, an access fault exception is triggered. The PMP has following features:

◇ Up to 16 regions can be configured;
◇ Read/Write/Execution memory protection;
◇ Minimum 4KB address range.

When TEE is configured, the PMP unit can import more scenarios according to the security of the core.

• Core Local Interrupt Controller (CLIC)

The E902 processor implements the RISC-V standard interrupt controller, CLIC and the CLINT. The CLIC has following features:

◇ Support up to 240 external interrupts;
◇ Up to 32 priority settings;
◇ Support level or positive/negative edge interrupt types;
◇ Support hardware vector interrupt;
◇ The control registers are memory mapped.

Debug Components

The E902 processor adopts T-Head customized 2-wire debug port or standard JTAG to communicate the host and E902 debug unit. The debug unit supports following operations:

- ◇ Support hardware/software breakpoint;
- ◇ Support hardware watchpoint;
- ◇ Check and modify CPU register resource;
- ◇ Single step or multi step flexibly supported;
- ◇ Speed up program download through 2-wire debug port or standard JTAG port.

Interface

The E902 has two 32-bit AMBA3 AHB-Lite master bus to communicate with the external memory or peripheral IP which are instruction and system bus. The internal request can be allocated to either bus according to the address.

XuanTie MCU Enhanced Extensions (XME)

The E902 processor implements the XME to deliver more powerful features such as:

- ◇ Support NMI;
- ◇ Support Lockup;
- ◇ Support sleep and deep sleep;
- ◇ Support soft reset operation;
- ◇ Support configurable reset address through top port during integration;
- ◇ Extend four functional instructions besides the standard RV32EMC ISA as following:

ICACHE.IALL		ICACHE.IPA		C.SLLI	C.SRAI	C.SRLI	C.MV	C.LWSP
MUL	MULH	MULHSU	MULHU	C.SWSP	C.ADDI4SPN		C.SUB	C.LW
DIV	DIVU	REM	REMU	C.SWSP	C.ADDI16SP		C.XOR	C.LUI
BGE	CSRRS	FENCE.I	LUI	SLL	SRAI	XORI	C.BEQZ	C.LI
BEQ	CSRRCI	FENCE	LHU	SH	SRA	XOR	C.ANDI	C.JR
AUIPC	CSRRC	ECALL	LH	SB	SLTU	WFI	C.AND	C.JALR
ANDI	BNE	EBREAK	LBU	ORI	SLTIU	SW	C.OR	C.JAL
AND	BLTU	CSRRWI	LB	OR	SLTI	SUB	C.NOP	C.J
ADDI	BLT	CSRRW	JALR	MRET	SLT	SRLI	C.ADDI	C.EBREAK
ADD	BGEU	CSRRSI	JAL	LW	SLLI	SRL	C.ADD	C.BNEZ

RV32E RV32M RVC XuanTie Customized

Processor Configuration Options

The XuanTie E902 processor has configurable feature options which can be set during the integration.

Feature	Options
Architecture	RV32EC or RV32EMC
Hardware Multiplier	When RV32EMC is chosen, one cycle multiplier or shift-add multiplier
Security	T-Head TEE technology or not included
Instruction cache	Not included or 2KB/4KB/8KB
Interrupts	32/64/96/128/192/240
PMP	Not included or 2/4/8/16 regions
Hardware Breakpoint Number	2/4/6
Debug Port	T-Head 2-wire debug port or standard JTAG

Software Ecosystems

- ◇ Compiler, assembler, linker, debugger and binary tools are contributed to GNU and supported officially;
- ◇ QEMU is contributed and supported officially;
- ◇ Code size optimized runtime lib
- ◇ Integrated Development Environment (CDK);
- ◇ High speed of program download(~1.1MB/s).

PPA

Performance	1.55 DMIPS/MHz (O2) 2.69 Coremark/MHz (O3)
Frequency	150MHz@worst case
Area	12K gates@minimal core
Power	4 uW/MHz

TSMC 40nm, 9T, RVT
Configuration is RV32EC, excluding PMP/CACHE/CLIC, etc.